INTEGRATED CIRCUIT

AWM 1301

COMPLEMENTARY DATA LINE DRIVER

The AWM1301 is a MS1 integrated circuit which has been designed to drive a twisted pair transmission line, having a return circuit, with high speed digital information.

This unit when used in conjunction with the AWM1302 integrated circuit, will provide superior immunity within an electrically noisy environment. It is capable of providing 30 mA complementary logic outputs when both inputs are in the low state.

The input requirements of this integrated circuit are compatible with series 74 TTL logic.

A wired-OR function is available.

8 lead T05 Package.
Details on page 4.

APPLICATIONS

- Transmission of high speed digital information over long lines.
- Computer coupling to industrial processes over twisted lines.

FEATURES

- Compatible with series 74 TTL.
- Performance specified up to 3000 picofarads line capacity.
- Withstands transients short circuits.
- Excellent noise immunity.
- Wired-OR function is available.
- Output at high level if input drive failure occurs.
- To be used as a driver for the AWM1302 receiver.

GENERAL CHARACTERISTICS

Package	8 lead T05
Storage Temperature	−10 to + 140°C
Operating Temperature	−10 to + 70°C
Supply Voltage Range	+4.5 to + 5.5 volts
Maximum Input to any pin	+5.5 volts
Minimum Input to any pin	−0.5 volts
Logic Level Inputs	DTL/TTL compatible
Dissipation	140 mW (typical)

Designed and Manufactured in Australia by –
AMALGAMATED WIRELESS (AUSTRALASIA) LTD.
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Postal Address – A.W.V. Private Mail Bag Ermington, 2115.
Telegrams "Valves" Ermington, Telephone 638 0411

AWM 1301
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Supersedes Issue ——

SCHEMATIC CIRCUIT

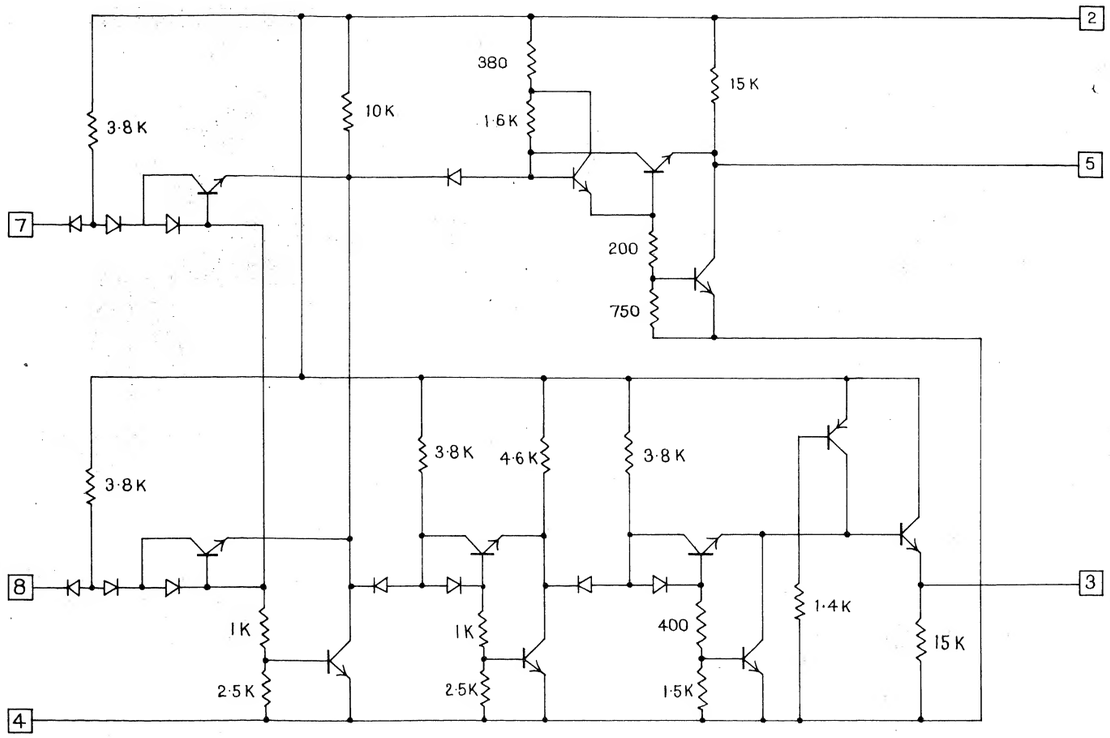
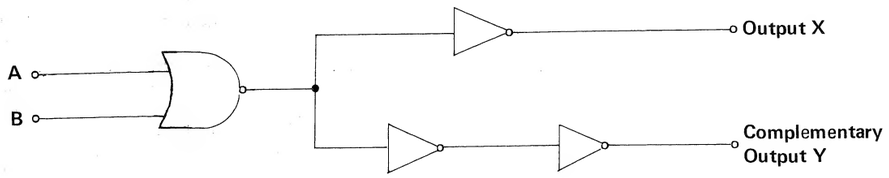


Figure 1. The resistance values shown in the circuit are nominal only.

LOGIC DIAGRAM



TRUTH TABLE

A	B	Complementary Output Y	Output X
H	H	L	H
H	L	L	H
L	H	L	H
L	L	H	L

STATIC ELECTRICAL CHARACTERISTICS

Pin	Function	Parameter (T_A=25°C)	Forcing Function	Limits Min.	Limits Typ.	Limits Max.	Units
2	Positive Supply	Voltage Vcc Current	 Vcc = 5.0V Both Inputs Open	4.5 12	5	5.5 3.0	V mA
3	Complementary Output Y	Low State Voltage (VOL) High State Voltage (VOH)	Vcc = 5.0V IL =-25mA IL =-100mA	 4.0 3.0		0.2	V V V
4	Ground						
5	Output X	High State Voltage (VOH) Low State Voltage (VOL)	Vcc = 5.0V IL = 25mA IL = 100mA	4.75	 1.0	5.0 0.4	V V V
7	Input A	High State Voltage (VIH) Current (IIH) Low State Voltage (VIL) Current (IIL)	 VIH = 5.0V VIL = 0.0V	2.0 0 −0.5	 −1.1	5.5 0.01 1.0 −1.5	V mA V mA
8	Input B	See pin 7.					

Note: Pins 1 and 6 are not connected.
All voltages with respect to ground (pin 4).

PROPAGATION DELAY TIMES

Propagation Delay	Y Output 30mA Sink	X Output 30mA Source	
td^+	65 n Sec.	75 n Sec.	typical
td^-	15 n Sec.	60 n Sec.	typical
td average	50 n Sec.	80 n Sec.	maximum

td average is the mean value of the positive and negative going propagation delays.

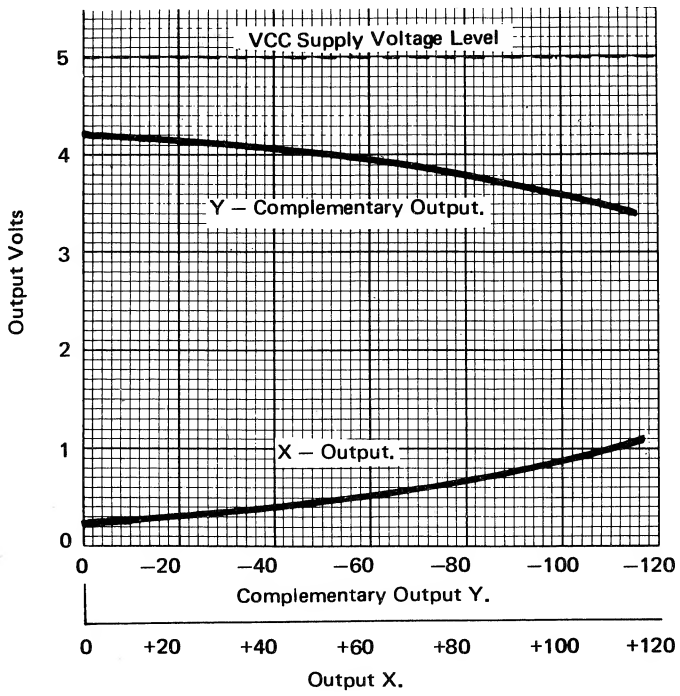


Figure 2. The typical output driving capability of the AWM1301 data line driver.

DIMENSIONAL OUTLINE AND PIN CONNECTIONS.

Pin No. 1. No connection.

2. Positive supply.

3. Complementary Output Y.

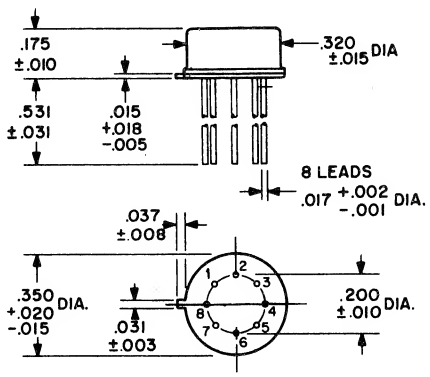
4. Ground and Case.

5. Output X.

6. No connection.

7. Input A.

8. Input B.



Dimensions in Inches